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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,010	07/22/2003	Kevin Weaver	100-22400 (PO5620)	8431

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/625,010	WEAVER ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 19-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 21* is/are rejected.

7)☒ Claim(s) *2-10,19,20 and 22-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 07/22/2003 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Invention II, claims 1-10 and 19-20, and cancellation of Invention II, claims 11-8, in the reply filed on 12/20/2004 is acknowledged. In the same reply, Applicant added claims 21-28 to Invention II. Accordingly, **claims 1-10 and 19-28** are present for examination.

Specification

3. Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were

permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(e) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(f) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(g) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(h) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification

should refer to another patent or readily available publication which adequately describes the subject matter.

(i) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(j) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(k) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

In the instant case, the Background of the Invention section and the Brief Summary of the Invention section appear to be missing.

Correction is required.

Claim Rejections

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall

have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim Rejections - 35 USC § 102

4. **Claims 1 and 21** are rejected under 35 U.S.C. 102(e) as being anticipated by Kolachina et al. U.S. Patent Application Publication 20050012512 (the '512 publication).

The '512 publication discloses in the Fig. 2, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device comprising:

a die ("integrated circuit" 200) having:

a semiconductor substrate (the bottom layer(s), no number);

a plurality of device conductive regions formed in and over the substrate; and

an interconnect structure (generally defined by metal lines 210,215 – paragraph [0030] - and the dielectric structure 220 that contacts the substrate) formed on the substrate to make electrical connections with the device conductive regions, and form a top surface of the die, the interconnect structure including:

a dielectric structure (220) that contacts the substrate; and

a plurality of layers of metal (210,215) that are formed in and isolated by the dielectric structure, each metal layer having a plurality of metal traces; and

a conductive region (connection pads, not shown, but must be present for the device to function, as detailed below in paragraph numbered 5) formed over the top surface of the die above the plurality of layers of metal.

Referring to **claim 21** and using the same reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the reference discloses a semiconductor device comprising:

a die having:

a semiconductor substrate;

a plurality of conductive regions formed in and near the substrate; and

an interconnect structure having a nonconductive top surface (of the dielectric structure 220), and a bottom surface that contacts the substrate, the interconnect structure having:

a dielectric structure,

a plurality of metal interconnects (such as metal lines 210-215 and the conductive plugs that connect them together) formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of conductive regions, and

a plurality of pads (connection pads, not shown, but must be present for the device to function, as detailed below in paragraph numbered 5) that contact the top surface, the plurality of pads being (inherently) electrically connected to the conductive regions (for the device to function).

Claim Rejections § 102 & § 103

5. **Claims 1 and 21** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Sakiyama et al. U.S. Patent Application Publication 20020079591 (the '591 publication).

The '591 publication discloses in the Fig. 3, and respective portions of the specification a semiconductor device as claimed or substantially as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device comprising:

a die (chip 1) having:

a semiconductor substrate (50);

a plurality of device conductive regions (not shown, paragraph [0051]) formed in and over the substrate; and

an interconnect structure (generally defined by wiring levels 53/54 and the dielectric structure (no number) that contacts the substrate 50) formed on the substrate (note also that "on" is relative, as the chip 1 is "flipped") to make electrical connections with the device conductive regions, and form a top surface of the die, the interconnect structure including:

a dielectric structure (no number) that contacts the substrate; and

a plurality of layers (wiring 53, 54) of a conductive material that are formed in and isolated by the dielectric structure, each conductive material layer having a plurality of conductive material traces; and

a conductive region (such as connection pads 51e) formed over the top surface of the die above the plurality of layers of conductive material layers.

Referring to **claim 21** and using the same reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the reference discloses a semiconductor device comprising:

a die having:

a semiconductor substrate;

a plurality of conductive regions formed in and near the substrate; and

an interconnect structure having a nonconductive top surface (the "top" surface of the no-number dielectric structure, which is inherently nonconductive, mentioned above), and a bottom surface that contacts the substrate, the interconnect structure having:

a dielectric structure,

a plurality of conductive material interconnects (such as wirings 53, 54 and plugs 54e) formed within the dielectric structure, the conductive material interconnects making electrical connections with the plurality of conductive regions, and

a plurality of pads (such as connection pads 51e) that contact the top surface, the plurality of pads being electrically connected to the conductive regions (as is evident from the figure and from the disclosure and as is known in the art) via the conductive material interconnects.

However, the reference does not explicitly teach that the conductive material is a metal as claimed.

Nevertheless, at the time the invention was made, the use of a metal, such as copper or aluminum, for the so-called interlevel metalization layers – which are called "wirings" by the reference and which are termed variously as "plurality of layers of metal" and "plurality of metal interconnects" in the claims – is widely known in the art and as is proved by the references cited

above and below. Therefore, if the reference's conductive material happens to be metal, the reference anticipates the claims; on the other hand, if the reference's conductive material is a non-metal conductive material, it would only require routine skill in the art, and therefore would have been obvious to one of ordinary skill in the art the time the invention was made, to change the reference's unspecified conductive material to a conductive metal, since the use of metal for a conductive material is widely known in the art. In addition, especially in the instant case, the use of metal conductors and the use of unspecified-material conductors are functionally equivalent, therefore the change from one to another would have been obvious and therefore not patentable.

In addition, the '591 publication is cited mainly to prove that, at the time the invention was made, every semiconductor die, semiconductor chip, or semiconductor integrated circuit inherently comprise a "a conductive region formed over the top surface of the die above" the (plurality of) layer(s) of conductive layers and every semiconductor die and semiconductor chip inherently comprises a plurality of connection pads that contact the top surface, the plurality of connection pads being electrically connected to the conductive regions via the conductive interconnect(s), for the every semiconductor die, semiconductor chip, or semiconductor integrated circuit to function.

6. **Claims 1 and 21** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Chandler U.S. Patent 6,211,527 (the '527 patent, cited by Applicant).

The '527 patent discloses in the figures, particularly Fig. 13, and respective portions of the specification a semiconductor device as claimed or substantially as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device comprising:

a die ("integrated circuit" 290, Fig. 13) having:

a semiconductor substrate (294);

a plurality of device conductive regions formed in and over the substrate (the plurality of device conductive regions are not shown but must be present for the device to function in any practical sense; and they may be by chance formed in and over the substrate, in which case, the reference anticipates the claims. In the alternative, i.e., the device conductive regions are only formed in the substrate or only formed on the substrate, it would only require routine skill in the art, and therefore would have been obvious, to form the device conductive regions in and over the substrate to fully utilize the space provided by the substrate); and

an interconnect structure (generally defined by conductive elements 300, 352 and the dielectric structure 314 that contacts the substrate 294) formed on the substrate to make electrical connections with the device conductive regions, and form a top surface of the die, the interconnect structure including:

a dielectric structure (314) that contacts the substrate; and

a plurality of layers of metal (portions of conductive elements 300, which are formed of copper or aluminum, column 12, lines 30-35) that are formed in and isolated by the dielectric structure, each metal layer having a plurality of metal traces; and

a conductive region (connection pads, not shown, but must be present for the device to function, as detailed above in paragraph numbered 5) formed over the top surface of the die above the plurality of layers of metal.

Referring to **claim 21** and using the same reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the reference discloses a semiconductor device comprising:

a die having:

a semiconductor substrate;

a plurality of conductive regions formed in and near the substrate; and

an interconnect structure having a nonconductive top surface (of the dielectric structure 314), and a bottom surface that contacts the substrate, the interconnect structure having:

a dielectric structure,

a plurality of metal interconnects (such as conductors 300, 352, formed of copper or aluminum as cited above) formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of conductive regions, and

a plurality of pads (connection pads, not shown, but must be present for the device to function, as detailed above in paragraph numbered 5) that contact the top surface, the plurality of pads being (inherently) electrically connected to the conductive regions (for the device to function).

Allowable Subject Matter

7. **Claims 2, 19, and 22** and their respective dependent claims 3-10, 20, and 23-28, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor device having all exclusive limitations as recited in claims 1/2 (claims 1 and 2), 1/19, and 21/22, characterized in that the conductive region of claim 2 includes silicon, or that the conductive region of claim 19 is non-metallic, or that the first conductive structure of claim 22 is formed in the first opening and on the top surface to make an electrical connection with the test structure.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
February 19, 2005